CL-Q28-LR-20-27
Single-Mode QSFP28 100G BIDI 20km Transceiver
RoHS 6 compliant



Features

- Supports 100GBASE-LR BIDI
- Lane signaling rate 106.25Gb/s with PAM4
- Up to 20km transmission on SMF
- EML Laser and PIN receiver
- 4x25.78Gb/s with NRZ electrical interface (CAUI-4)
- Support KP4 FEC inside the module
- High speed I/O electrical interface
- I2C interface with integrated Digital Diagnostic monitoring
- QSFP28 MSA package with simplex LC connector
- Single +3.3V power supply
- Power consumption <3.5 W
- Operating case temperature: 0 to +70 °C
- Compliant to 802.3cu, SFF-8636&SFF-8679 standard
- Compliant to 100G Lambda MSA 100G-LR1 Optical Specifications
- Complies with EU Directive 2015/863/EU

Applications

- 100 Gigabit Ethernet
- Data Center

PART NUMBER	Monitor	INPUT/OUTPUT	SIGNAL DETECT	TEMPERATURE
CL-Q28-LR4-20-27	X	AC/AC	TTL	0°C to 70 °C

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DESCRIPTIONS

The 100G QSFP28 LR1 BIDI is designed for 20km optical communication applications. It is intended for the service with single mode fiber in 100Gb/s high speed data communications. The optical signals are multiplexed to a single-mode fiber through commercial standard LC connector.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	T_S	-40	-	+85	°C	
Supply Voltage	V_{CC}	-0.5	-	+4.0	V	
Operating Relative Humidity	RH	-	-	+85	%	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_C	0	-	+70	°C	
Power Supply Voltage	V_{CC}	3.13	3.3	3.47	V	
Transmission Distance	TD	-	-	20	km	Over SMF

Optical and Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter						
Center Wavelength	CW	1264.5	1271	1277.5	nm	
		1324.5	1331	1337.5	nm	
Signaling Rate	SR			53.125	GBd	
Frequency Offset	Foffset	-100		100	ppm	
Average Launch Power	PTX	-0.2	-	6.6	dBm	1
Transmitter and dispersion eye closure for PAM4 (TDECQ) (max)	TDECQ	-	-	3.6	dBm	
Average Output Power (Laser Turn off)	Poff	-	-	-30	dBm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Extinction Ratio	ER	3.5	-	-	dB	
RIN_OMA	RIN	-	-	-136	dB/Hz	
Transmitter reflectance	Tref	-	-	-26	dB	
Optical Return Loss Tolerance	ORLT	-	-	15.6	dB	
Receiver						
Center Wavelength	CW	1324.5	1331	1337.5	nm	
		1264.5	1271	1277.5	nm	
Damage threshold	Pdamage	7.6	-	-	dBm	2
Average Rx Power	PRx	-10	-	6.6	dBm	3

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Receive power _OMAouter	POMA	-	-	6.8	dBm	
Receiver sensitivity _OMAouter for TDECQ < 1.4 dB for 1.4 dB ≤ TDECQ ≤ 3.4 dB	SEN _OMA	-	-	-7.6 –9 +TDECQ	dBm	4
Reflectance	Ref	-	-	-26	dB	
Los Assert	LosA	-26	-		dBm	
Los De-Assert	LosDA	-	-	-10	dBm	
Los Hysteresis	LosH	0.5	-	-	dB	
Stressed receiver sensitivity _OMAouter	SRS	-	-	-5.4	dBm	5
Conditions of stressed receiver sensitivity teste :						
Stressed eye closure for PAM4 (SECQ)				3.6	dB	6

Notes:
1. The optical power is launched into SMF.
2. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
3. Average receive power, each lane (min) is informative and not the principal indicator of signal strength.
4. Measured with conformance test signal at TP3 using the test pattern PRBS31Q or scrambled idle for stressed receiver sensitivity for the BER= 2.4x10-4.
5. Measured with conformance test signal at TP3 (see3.11) for the BER specified in IEEE Std 802.3cu
6. Ceq is a coefficient defined in IEEE Std 802.3-2022 clause 121.8.5.3 which accounts for reference equalizer noise enhancement.

Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Transmitter (Module Input)						
Input Differential Impedance	Rin	-	100	-	Ohm	
Differential Data Input Amplitude	$V_{IN,P-P}$		-	900	mVpp	
Differential termination mismatch (max)	D-mismatch	-	-	10	%	
DC common-mode input voltage		-0.3	-	2.8	V	
Transition time(20%~80%)	Tr Tf	10	-	-	ps	
LPMode, Reset and ModSelL / Tx dis	V_{IL}	-0.3	-	0.8	V	
LPMode, Reset and ModSelL / Tx dis	V_{IH}	2.0	-	V_{CC}+0.3	V	
Receiver (Module Output)						
Output Differential Impedance	Rout	-	100	-	Ohm	
Differential Data Output Amplitude	V_{OUTP-P}	-	-	900	mVpp	
Differential termination mismatch (max)	D-mismatch	-	-	10	%	
Transition time, 20% to 80%	Tr Tf	12	-		ps	
ModPrsL and IntL/ Rx los	V_{OL}	0	-	0.4	V	
ModPrsL and IntL/ Rx los	V_{OH}	V_{CC}-0.5	-	V_{CC}+0.3	V	

Digital Diagnostics

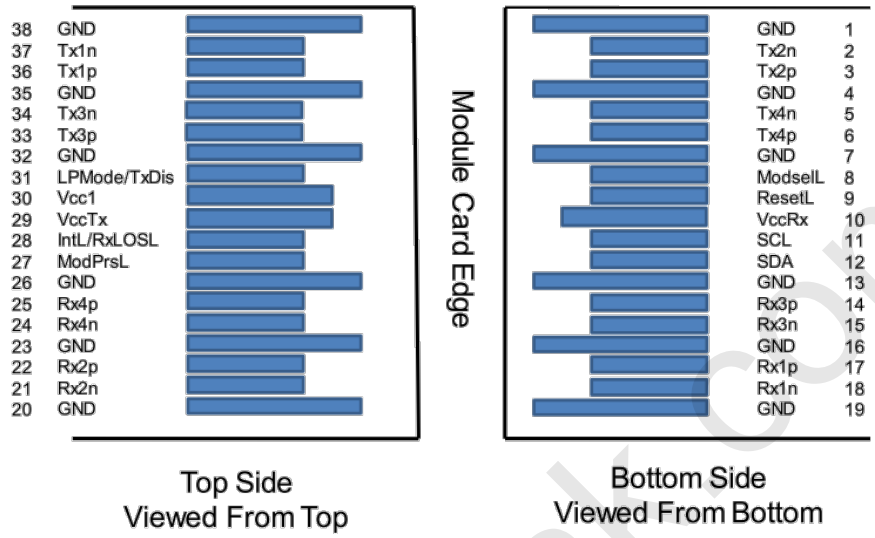
Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to Vcc	±3%	V	Internal
Tx Bias Current	0 to 100	±10%	mA	Internal
Tx Output Power	-0.2 to 6.8	±3	dB	Internal
Rx Input Power	-10 to 7.6	±3	dB	Internal

Communication Interface Timing Characteristics

Parameter	Symbol	Min	Max	Unit	Calibration	Notes
Initialization time	t_init		10	s	Time from power on or hot plug until the module is fully functional. This time applies to Power Class 2 or higher modules when LPMode is pulled low by the host, and to all Power Class 1 modules.	Room Temperature
LPMode Assert Time	ton_LPMode		100	ms	Time from when the host releases LPMode to high until module power consumption reaches Power Class 1.	
Rx LOS Assert Time	ton_LOS		100	ms	Time from Rx optical signal loss to Rx LOS bit set to 1 and IntL pulled low by the module.	
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set to 1 and IntL pulled low by the module.	
Tx Disable Deassert Time	toff_TxDis		400	ms	Time from Tx Disable bit cleared to 0 until optical output rises above 90% of nominal.	
Tx Disable Assert Time	ton_TxDis		100	ms	Time from Tx Disable bit set to 1 until optical output falls below 10% of nominal.	

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Pin Diagram



Pin Definitions

PIN	Logic	Symbol	Description	Plug Seq.	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTLL-I	ModSelL	Module Select	3	
9	LVTLL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3	
13		GND	Ground	1	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1

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17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/Rx_LOS	Interrupt/Rx_LOS	3	3
29		VccTx	+3.3 V Power Supply transmitter	2	2
30		Vcc1	+3.3 V Power Supply	2	2
31	LVTTL-I	LPMode/TxDIS	Low Power Mode/Tx_Disable	3	3
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Notes:
1. GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in MSA. The connector pins are each rated for a maximum current of 1000 mA.
3. Two Multi-Purpose Pin for supporting Tx_DIS and Rx_LOS function in the 100G QSFP28 LR1 BIDI module.

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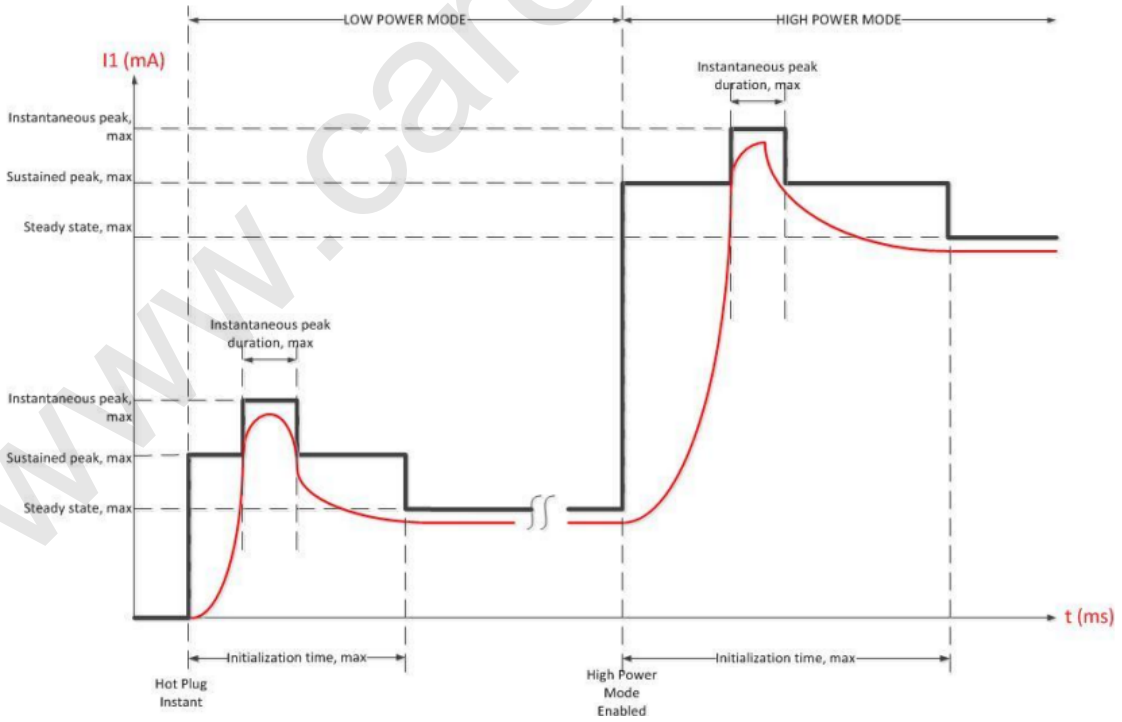
Partly Management Interface

Page	Byte	Bit	Name	Description
00h	99	1	LP/TxDis ctrl	LPMode/TxDis input signal control. See SFF8679 for a complete description. 0b = LPMode 1b = TxDIS
		0	IntL/LOSL ctrl	IntL/LOSL output signal control. See SFF-8679 for a complete description. 0b = IntL 1b = LOSL

Module Power Supply Specification

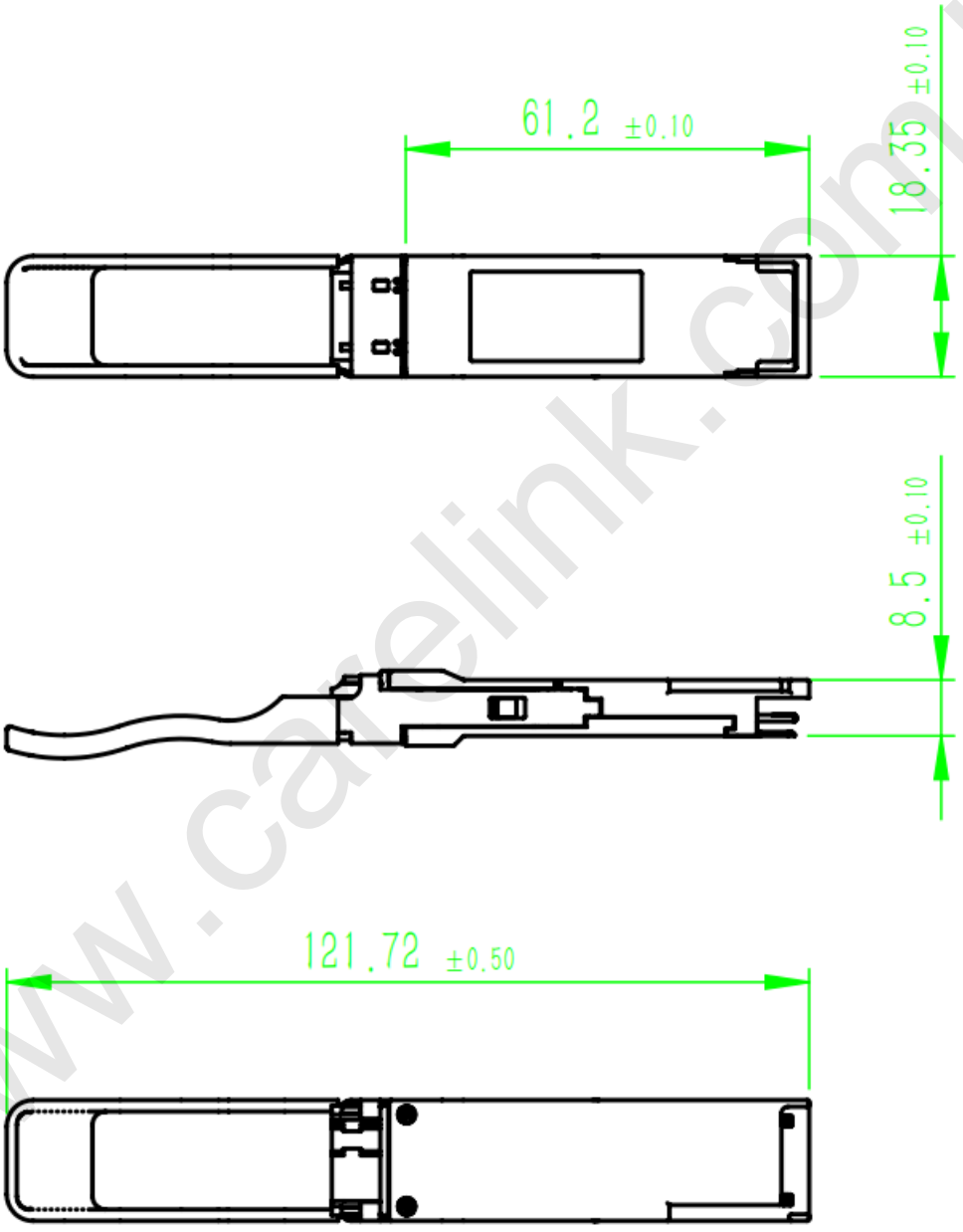
100G QSFP28 LR1 BIDI needs power supply of 3.3V , the following figure shows the timing of the initial module turn-on in Low Power Mode, and the later transition to full power mode after the host system has enabled it via the two-wire interface. And shows the power supplies to the module and the according current values. Module power supply refer to SFF-8679 TABLE 5-6.

100G QSFP28 LR1 BIDI INRUSH CURRENT TIMING



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Mechanical Diagram



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