CL-CF2-Q28
CFP2 to QSFP28 Adapter
RoHS 6 compliant

Features

- CAUI -4 Electrical Interface:4 Lanes @25.78Gbit/s for CFP2 port
- CAUI -4 Electrical Interface:4 Lanes @25.78Gbit/s for QSFP28 port
- Hot Pluggable
- MDIO, I2C Support
- Compliant to CFP2 MSA
- RoHS-6 compliant
- Case operating temperature: 0 to 70 °C
- The CL-CFP2-QSFP28 Adaptor

Module converts a 100 Gigabit CFP2 port into a 100 Gigabit QSFP28 port. With the Adaptor Module, customers have the flexibility to use the 100 Gigabit CFP2 interface port of a switch with CFP2 modules or QSFP28 modules.

Applications

- 100GBASE-LR4&LR4 Lite (Adapter+QSFP28-LR4&LR4 Lite); 100GBASE-SR4(Adapter+QSFP28-SR 4);
- 100GBASE-ER4&ER4 Lite (Adapter+QSFP28-ER4&ER4 Lite);
- Data aggregation and backplane applications;
- High-speed core router connections& Datacom/Telecom

PART NUMBER	Monitor	INPUT/OUTPUT	SIGNAL DETECT	TEMPERATURE
CL-CF2-Q28	X	AC/AC	TTL	-5°C to 70 °C
CL-CF2-Q28i	X	AC/AC	TTL	-40°C to 85 °C

Absolute Maximum Ratings

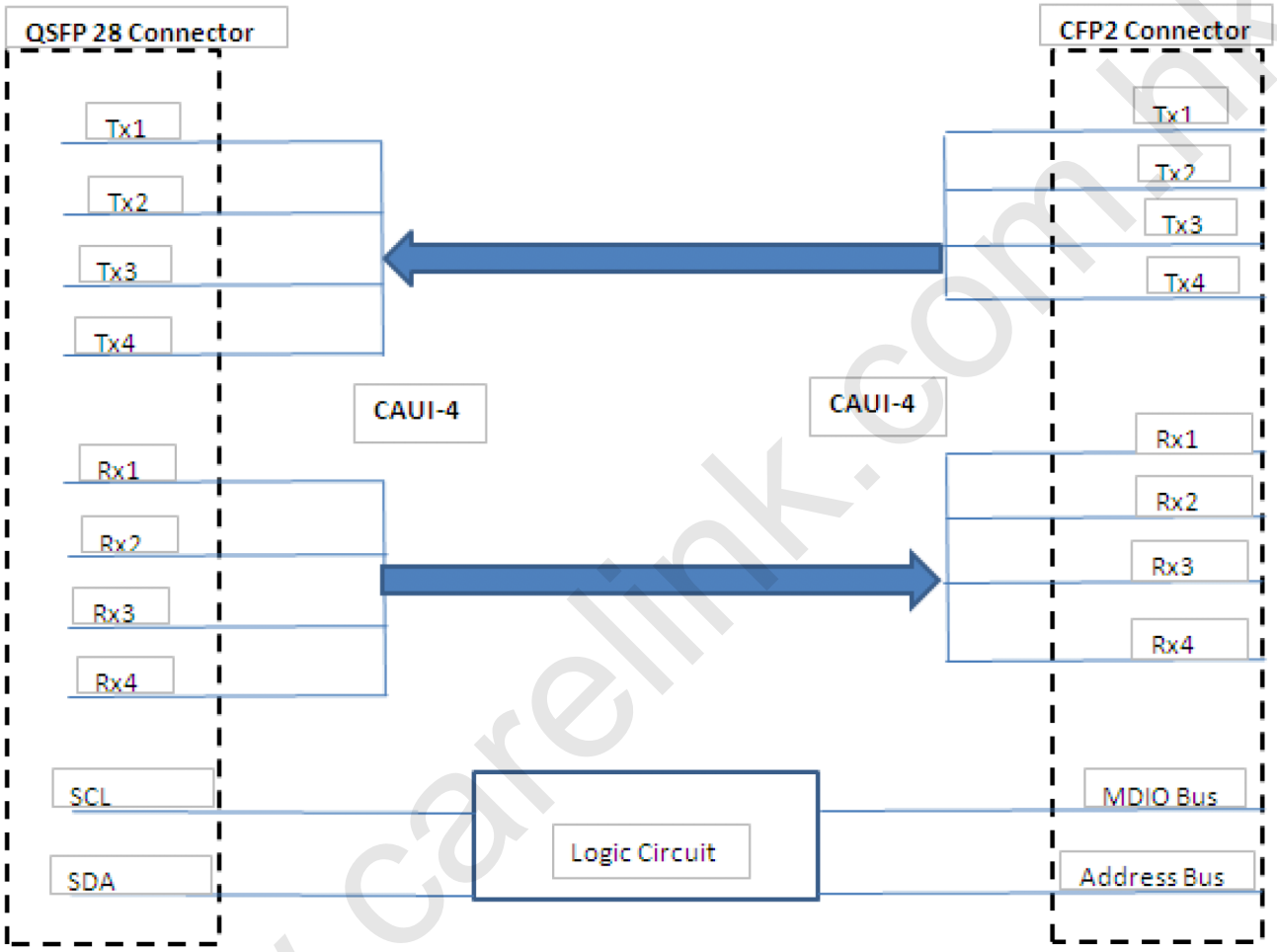
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Storage Temperature	TS	-40	-	+85	°C	
Supply Voltage	VCC	-0.5	-	+4.0	V	
Operating Relative Humidity	RH	-	-	+85	%	

CAUI-4 Interface (QSFP28 port&CFP2 port)

CAUI Receiver Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Signal Rate Per Lane			25.78		Gb/s	
Differential data output swing per lane	Vout,pp	CAUI-4 as defined by IEEE P802.3bm			mV	
Data output rise time	tr				ps	
Data output fall time	tf				ps	

CAUI Transmitter Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Signal Rate Per Lane			25.78		Gb/s	
Frequency offset		-100		100	ppm	100G Ethernet
		-20		20	ppm	OTU4
Input differential impedance	Rin	CAUI-4 as defined by IEEE P802.3bm			Ω	
Differential data input swing per lane	Vin,pp				mV	
Data input rise time tolerance	tr				ps	
Data input fall time tolerance	tf				ps	

Block Diagram



Recommended Interface Circuit

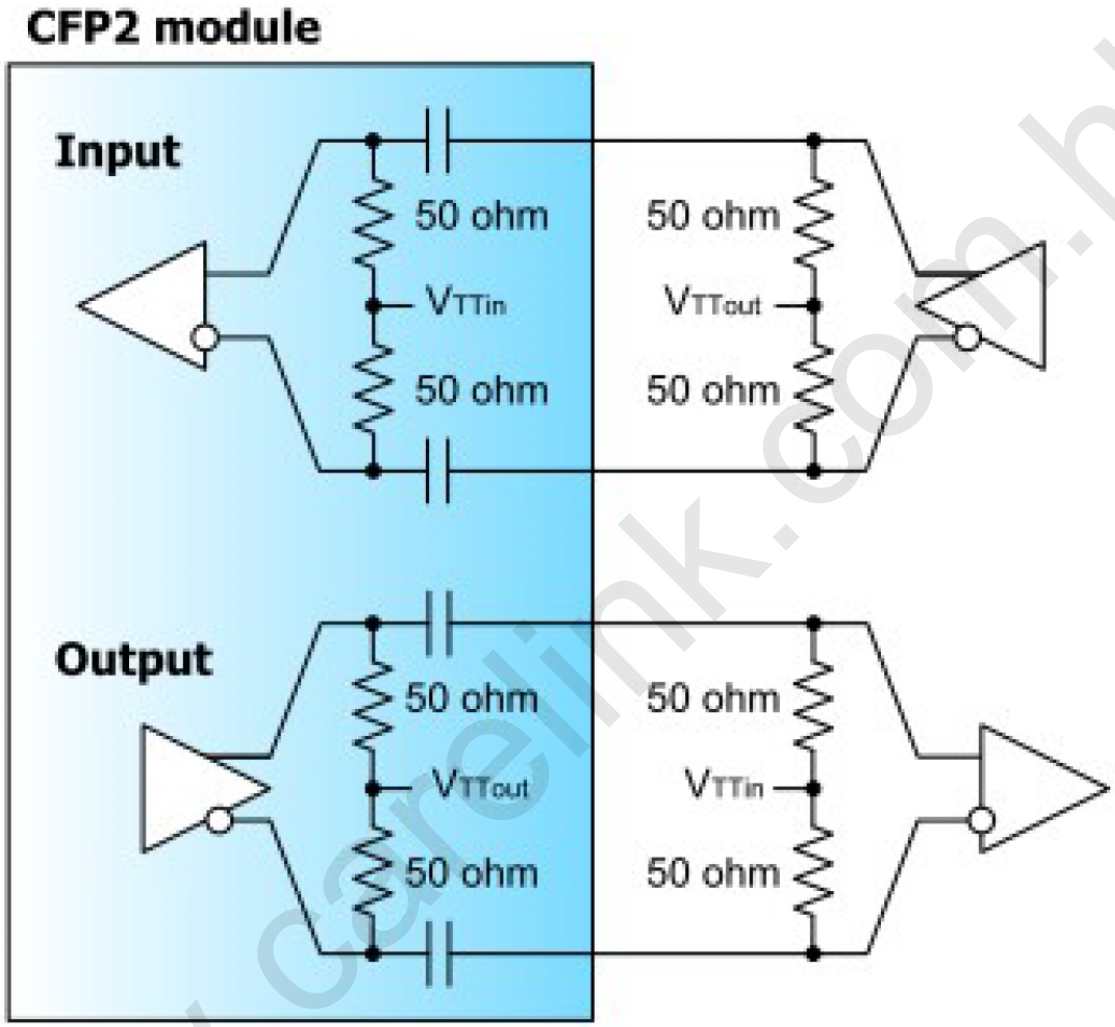


Figure 1. Recommended High Speed I/O for Data and Clocks

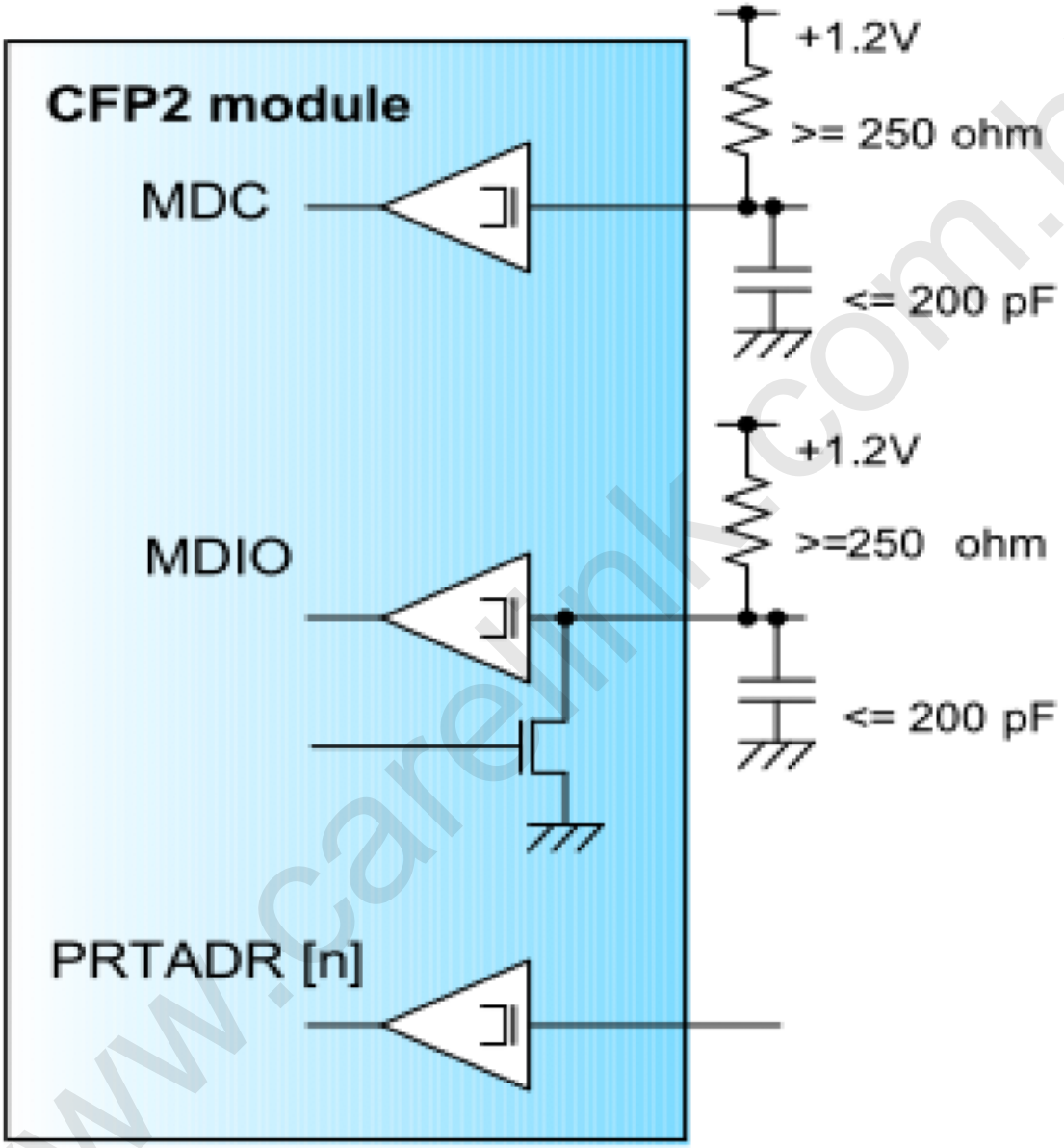
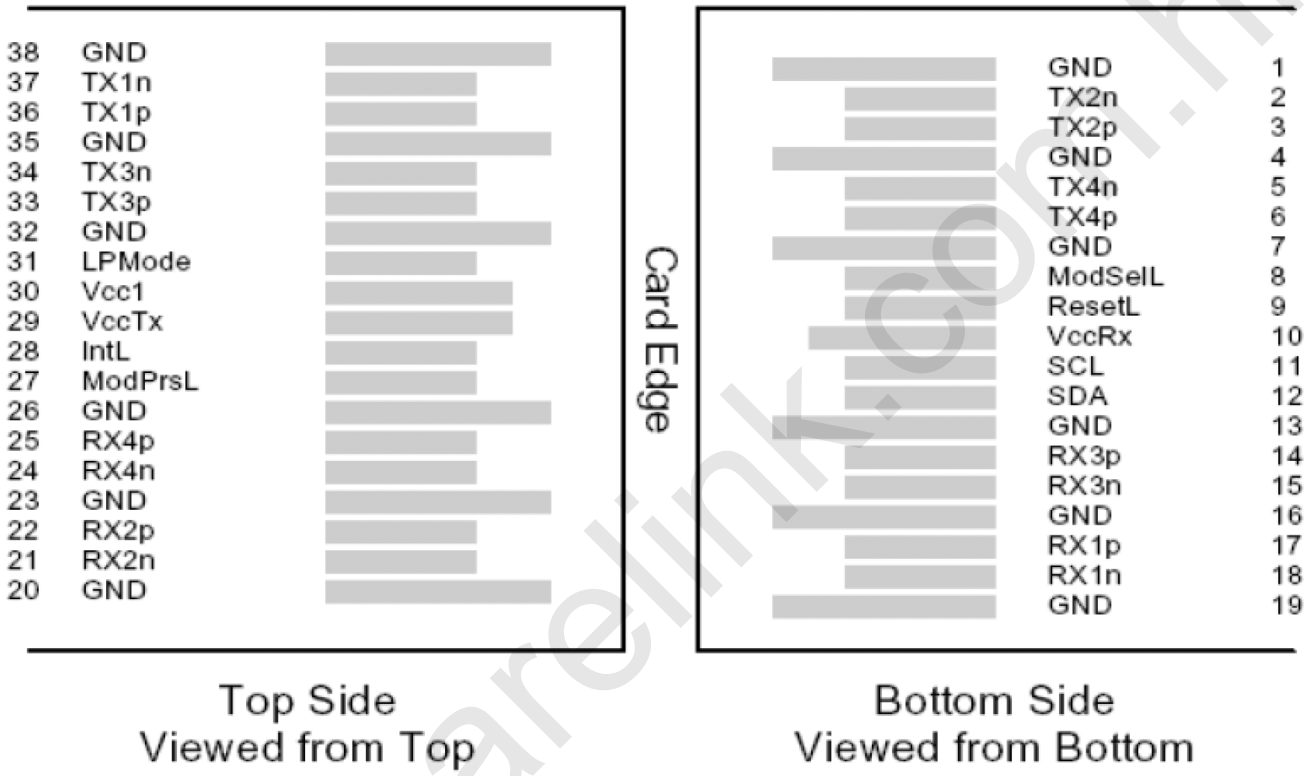
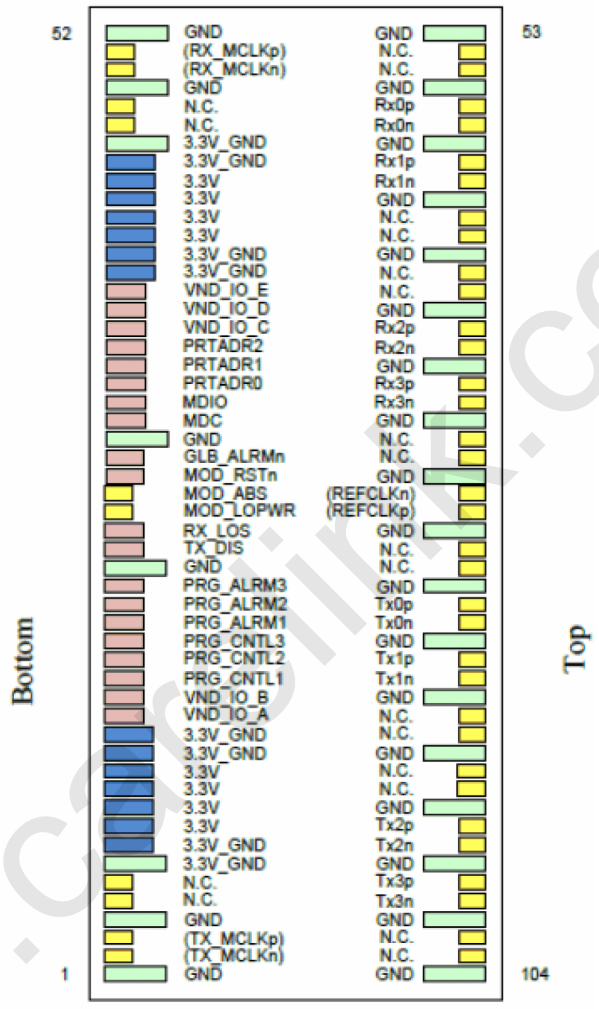


Figure 2 Recommended MDIO Interface Termination

PIN Assignment of QSFP28 port



PIN Assignment of CFP2 port



Pin Definition

PIN	Name	I/O	Logic	Description
1	GND			
2	(TX_MCLKn)	O	CML	Not Support
3	(TX_MCLKp)	O	CML	Not Support
4	GND			
5	N.C			No Connect
6	N.C			No Connect
7	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V_GND			
9	3.3V			3.3V Module Supply Voltage
10	3.3V			3.3V Module Supply Voltage
11	3.3V			3.3V Module Supply Voltage
12	3.3V			3.3V Module Supply Voltage
13	3.3V_GND			
14	3.3V_GND			
15	VND_IO_A	I/O		Module Vendor I/O. Must No Connect at host board
16	VND_IO_B	I/O		Module Vendor I/O. Must No Connect at host board
17	PRG_CNTL1	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used
18	PRG_CNTL2	I	LVCMOS w/ PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤3W, "01":≤6W, "10": ≤9W,
19	PRG_CNTL3	I	LVCMOS w/ PUR	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤3W, "01":≤6W, "10": ≤9W,
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0":module not high powered up
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO, MSA Default:MOD_READY,
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
23	GND			
24	TX_DIS	I	LVCMOS w/ PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled

25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
				Module Low Power Mode. "1" or NC: module in low power (safe) mode,
				Module Absent. "1" or NC: module absent, "0":module present,
			LVCMOS	Module Reset. "0" resets the module, "1" or NC =module
				Global Alarm. “0": alarm condition in any MDIO Alarm
30	GND			
31	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
32	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
33	PRTADR0	I	1.2V	MDIO Physical Port address bit 0
34	PRTADR1	I	1.2V	MDIO Physical Port address bit 1
35	PRTADR2	I	1.2V	MDIO Physical Port address bit 2
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
39	3.3V_GND			
40	3.3V_GND			
41	3.3V			3.3V Module Supply Voltage
42	3.3V			
43	3.3V			

44	3.3V			
45	3.3V_GND			
46	3.3V_GND			
47	N.C			No Connect
48	N.C			No Connect
49	GND			
50	(RX_MCLKn)	O	CML	Not Support
51	(RX_MCLKp)	O	CML	Not Support
52	GND			

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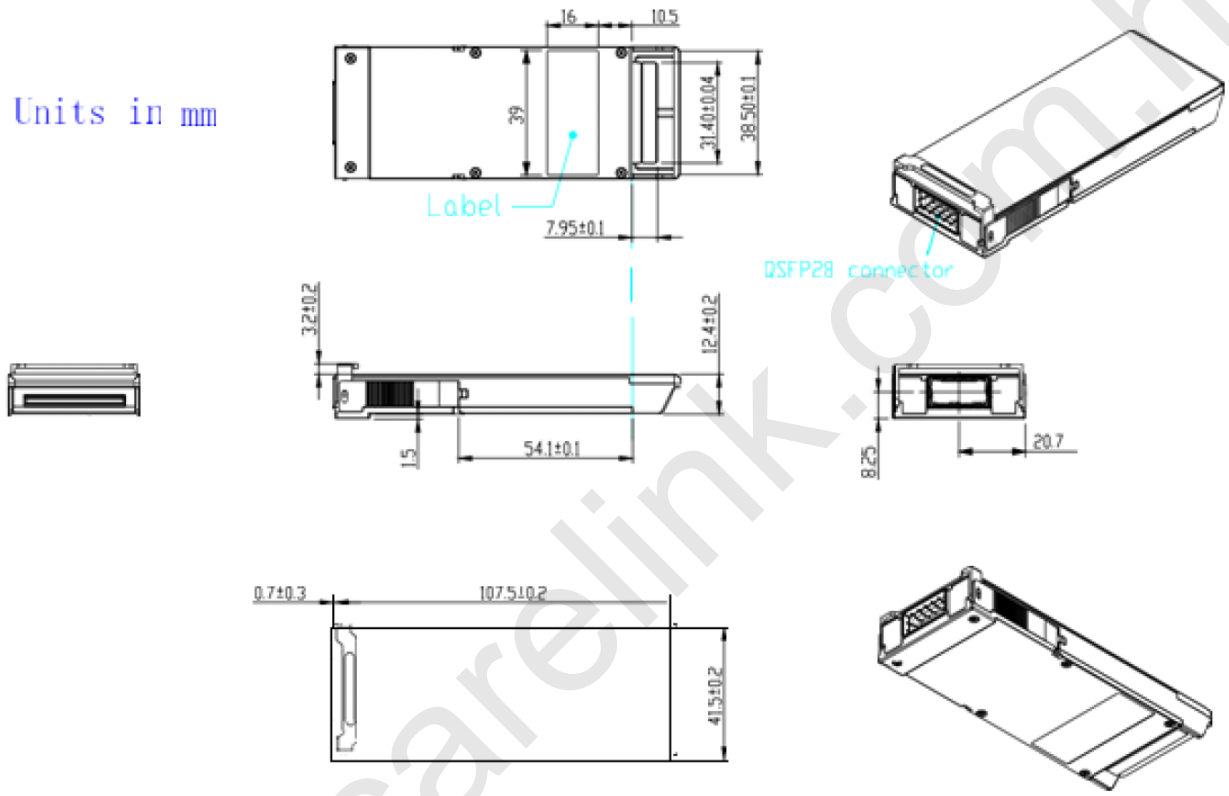
Package Outline (Unit:mm)



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