CL-CF2-DCO-XX-XXXX
Coherent CFP2 Transceiver / 100G/200G CFP2 DCO MR
RoHS 6 compliant

Features

- Support Flex-grid channel spacing DWDM infrastructure
- Support Flexible client-side interfaces:100GbE, OTU4
- Support OpenROADM(oFEC) line-side FEC types for 100G/200G(31.57GBaud)
- Framed PRBS generator/checker on the host and network side interfaces
- Network and client loopback at the near-endian and far-endian point
- CFP MSA IEEE802.3 Clause 45 compliant MDIO
- 104pin CFP2 MSA compliant connector
- Hot Swappable
- RoHS compliant

PART NUMBER	Monitor	INPUT/OUTPUT	SIGNAL DETECT	TEMPERATURE
CL-CF2-DCO-ZR-100	X	AC/AC	TTL	-5°C to 70 °C
CL-CF2-DCO-ZR-100i	X	AC/AC	TTL	-40°C to 85 °C
CL-CF2-DCO-MR-1200	X	AC/AC	TTL	-5°C to 70 °C
CL-CF2-DCO-MR-1200i	X	AC/AC	TTL	-40°C to 85 °C
CL-CF2-DCO-MRS-2000	X	AC/AC	TTL	-5°C to 70 °C
CL-CF2-DCO-MRS-2000i	X	AC/AC	TTL	-40°C to 85 °C

Module Description

The Module uses a 104-pin OIF CFP2 Hardware Specification connector for all electrical interfaces with the host card, whereas the optical interfaces on the line side are provided through the optical receptacles on the CFP2. The module can be portioned into three functional parts: Tx path, Rx path and Control & Power block.

Path Description

The host interface is comprised of a total of 8 high-speed SerDes lanes. This allows module to support two interfaces for 100G or 200G application: an independent double 4-Lane mode client interfaces (for 1*100GbE/2*100GbE, 1*OTU4/2*OTU4 application).

Module Configuration

The module is designed to maximize the number of use-cases in which it can be deployed. Both the host interface as well as the network interface can be configured for different applications.

Typical Application

The application field of the module is widely used from short haul (ZR) to Metro (MR) and Data Center Interconnection (DCI). As shown in Figure 1, it is comprised of high-data lanes, a single 3.3V power supply, an MDIO interface for module control and status report, and dedicated alarm and control pins (not shown on the figure 1).

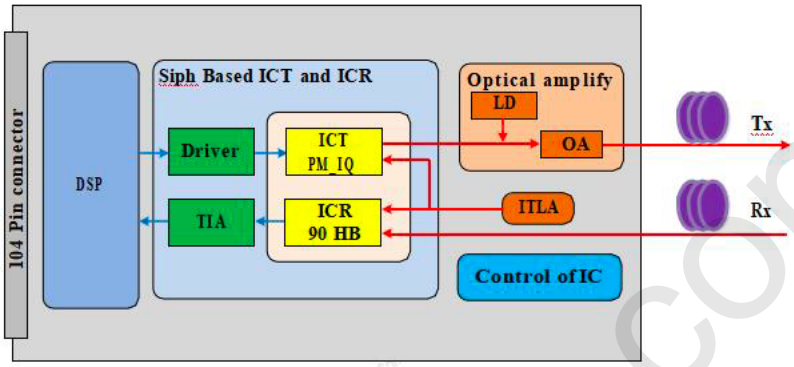

Figure1:Functional diagram of Module

Host Interface

The table1 summarizes the supported client and interface modes in the host interface. The electrical properties of the host interface are discussed in detail in section 3.

Table1:Client interface

Applications	Client Side type	Client I/F mode	Client lane rate(Gb/s)	Note
1*100G	1*CAUI-4	4*25Gbps(NRZ)	For 100G	
1*OTU4	1*OTL4.4	4*28Gbps(NRZ)	For 100G	
2*100G	2*CAUI-4	8*25Gbps(NRZ)	For 200G	
2*OTU4	2*OTL4.4	8*28Gbps(NRZ)	For 200G	

The host rate is dependent on the framing type and the supported host rates are shown in the following table.

Table2:Host Rates

Application	Host Frame	Host Data Bit Rate(Gbps)	Offset(ppm)	Singal
1*100G	1*103.125	100	Ethernet class	1*100G
1*OTU4	1*111.8099736	20		1*OTU4
2*100G	2*103.125	100	Ethernet class	2*100G
2*OTU4	2*111.8099736	20		2*OTU4

FEC mode

Line/network side FEC: the module offers two ways of protecting the payload using forward error correction.
The information of FEC mode and modulation mode is as following table.
Table3:Line FEC Type and modulation mode

Application	Modulation	FEC Type	Lane Baud	Grid	OSNR	Note
100G	DP-QPSK	oFEC	31.57G	50G	11.5	
200G	DP-16QAM	oFEC	31.57G	50G	19.5	

Absolute maximum ratings

The absolute maximum ratings given in the table below define the damage thresholds. Hence, the component shall withstand the given limits without any irreversible damage.

Table4:Absolute Maximum Ratings

Parameter	Condition (1)	Min	Max	Unit
Storage Temperature Range		-40	85	℃
Storage Humidity	Relative, no-Condensing	-	85	%
Case Temperature Range		-5	+75	℃
Power supply		-0.3	3.7	V
Input power(Optical)	Peak Power		10	dBm

Note:Top=25℃ , unless otherwise specified.

Operating conditions

Table5:Operating Environment

Parameter	Condition	Symbol	Min	Max	Unit
Operating Case Temperature (Top)		Tcase	-5	70	℃
Relative humidity Range	Non-condensing	RH	-	85	%
Operating Input Optical Power of Signal		Psig	-18	+5	dBm
Storage Temperature Range			-40	85	℃

Power supply

Table6:Power specifications

Parameter	Condition	Min	Typ	Max	Unit
3.3V DC Power Supply Voltage		3.2	3.3	3.4	V
3.3V DC Power Supply Current				8	A
Power Consumption	Low Power			2	W
Power Consumption @ DP-16QAM with oFEC for 200G			22	24	W
Power Consumption @ DP-QPSK with oFEC for 100G			18	21	W
Inrush current	Power class 5 & 6			300	mA/us
Turn-off current	Power class 5 & 6	-300			mA/us
Power Supply Noise	DC - 1MHz			2	%
Power Supply Noise	1 - 10MHz			3	%

Hardware Control Pins

The control and status reporting functions between a host and a CFP2 module use non-data control and status reporting pins on the 104-pin connector. The control and status reporting pins work together with the MDIO interface to form a complete HOST-CFP2 management interface. The status reporting pins provide status reporting. There are six (6) Hardware Control pins, five (5) Hardware Alarm pins, and six (6) pins dedicated to the MDIO interface. Specification of the CFP2 hardware signaling pins are given in Ref. [1] with the following changes listed in this section. The module supports real-time control functions via hardware pins, listed in table 7 as bellow.

Table7:Control Pins

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
17	PRG_CNTL1	Programmable Control 1 *MSA Default: TRXIC_RSTn, TX & RX ICs reset,* *"0": reset, "1"or NC: enabled*	I	3.3V LVCMOS	per CFP MSA MIS Ref. [7]		Pull – Up[2]
18	PRG_CNTL2	Programmable Control 2 *MSA Default: Hardware Interlock LSB*	I	3.3V LVCMOS			Pull – Up[2]
19	PRG_CNTL3	Programmable Control 3 *MSA Default: Hardware Interlock MSB*	I	3.3V LVCMOS			Pull – Up[2]
24	TX_DIS	Transmitter Disable	I	3.3V LVCMOS	Disable	Enable	Pull – Up[2]
26	MOD_LOPWR	Module Low Power Mode	I	3.3V LVCMOS	Low Power	Enable	Pull – Up[2]
28	MOD_RSTn	Module Reset, Active Low (invert)	I	3.3V LVCMOS	Enable	Reset	Pull – Down[3]

[2]Pull-Up resistor (4.7 kOhm to 10 kOhm) is located within the CFP2 module

[3]Pull-Down resistor (4.7 kOhm to 10 kOhm) is located within the CFP2 module

Hardware Alarm Pins

The CFP2 Module supports alarm hardware pins as listed in Table 8.

Table8:Alarm Pins

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
20	PRG_ALRM1	Programmable Alarm 1 *MSA Default: HIPWR_ON*	O	3.3V LVCMOS	Active High per CFP MSA MIS Ref. [7]		
21	PRG_ALRM2	Programmable Alarm 2 *MSA Default: MOD_READY, Ready state has been reached*	O	3.3V LVCMOS			
22	PRG_ALRM3	Programmable Alarm 3 *MSA Default: MOD_FAULT*	O	3.3V LVCMOS			
25	RX_LOS	Receiver Loss of Signal	O	3.3V LVCMOS	Loss of Signal	OK	
27	MOD_ABS	Module Absent	O	3.3V LVCMOS	Absent	Present	Pull Down[2]

Management Interface Pins

The CFP2 Module supports alarm, control and monitor functions via an MDIO bus. Upon module initialization, these functions are available. CFP2 MDIO electrical interface consists of six (6) pins including two (2) pins for MDC and MDIO, three (3) Physical Port Address pins, and the Global Alarm pin.

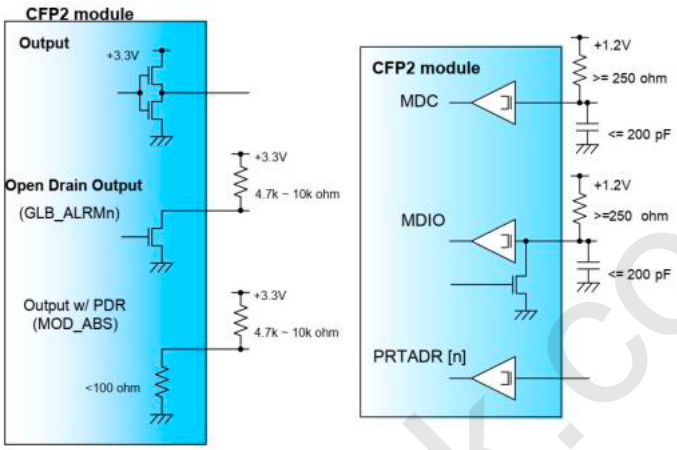

Figure 2: Reference +3.3V LVCMOS Output and MDIO Interface Termination

MDC is the MDIO Clock line driven by the host and MDIO is the bidirectional data line driven by both the host and module depending upon the data directions. The CFP2 MDIO pins are listed in Table 9.

Table9:Management Interface Pins (MDIO/MDC)

Pin #	Symbol	Description	I/O	Logic	"H"	"L"	Pull-up /down
29	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS	OK	Alarm	
31	MDC	MDIO Clock	I	1.2V LVCMOS			
32	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS			
33	PRTADR0	MDIO Physical Port address bit 0	I	1.2V LVCMOS	per CFP MSA MIS Ref. [7]		
34	PRTADR1	MDIO Physical Port address bit 1	I	1.2V LVCMOS			
35	PRTADR2	MDIO Physical Port address bit 2	I	1.2V LVCMOS			

Module Management Interface Description

The CFP2 module utilizes MDIO IEEE Std 802.3TM-2012 clause 45 for its management interface. The CFP2 MDIO implementation is defined in a separate document entitled, "OIF-CFP2-DCO-01.0, Revision 1.0, October 17, 2018". When multiple CFP2 modules are connected via a single bus, a particular CFP2 module can be selected by using the Physical Port Address pins.

High-Speed Electrical Specifications

The transmitter and receiver comply with the CEI-56G-VSR-PAM4 or CEI-28G-VSR electrical specification (OIF-CEI-04.0). The data lines are AC-coupled and terminated in the module per the following figure from the CFP2 MSA.

The Module high speed electrical interface supports the following configurations:

4 tx lanes + 4 rx lanes, each at 56Gbit/s or 28Gbit/s

8 tx lanes + 8 rx lanes, each at 28Gbit/s

Loopback

The module support loopback functionality. The host loopback (Loopback ○1) and the network loopback (Loopback ○2) are shown at bellowing figure. For details on controlling the loopback mode, please refer to Reference [1]. In optional loopback, TXn is looped back to RXn, for example TX0+ to RX0+, on both host and network side.

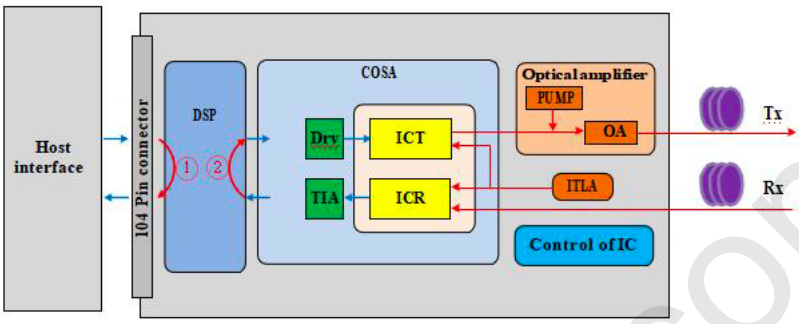

Figure 3: Module Loopback Orientation

Reference Clock

There is a local reference clock in this module, so the module don't need the external 1/160 or 1/32 reference clock which is came from the pin 78 and pin 79, the pins can be in disconnected status.

Optical Specifications

Unless noted all specifications given in this document are End-of-Life numbers and are valid over case temperature from -5℃ to +70℃.

Optical Transmitter Specifications

There are show all Transmitter specifications in the following table.

Table 10: Optical Transmitter Specifications

Parameter	Typ	Min	Max	Unit	Condition/comments
Transmitter Frequency Range	193.7	191.3	196.10	THz	C band 50GHz ITU-T grid. Frequency range over which thespecifications hold unless noted otherwise.
Channel Spacing	50			GHz	
Frequency Stability		-2.5	2.5	GHz	Frequency stability relative to ITU grid.
Frequency Offset		-2.5	2.5	GHz	
Frequency Fine Tuning Range		-6.0	6.0	GHz	
Fine Tuning Resolution	100			MHz	
Channel Tuning Speed			80	s	
Line Width			500	kHz	FWHM
SMSR (Side mode suppression Ratio)	45	40		dB	Measured over +/-2.5nm range around the target frequency with0.06nm RBW without modulation.
Transmitter output power range	0	-5	+5	dBm	Transmitter output is settable in steps of 0.1 dB at any power levelwithin the specified frequency range
Output power stability		-0.5	0.5	dB	Difference over temperature, time, wavelength and aging.
Output power monitor accuracy		-2	2	dB	Difference between the set value and actual value over aging.
Transmitter turn-up time from warm start		-	15	ms	Module is in Ready state. The maximum transmitter turn-up time iscounted from de-assert the Tx_disable Pin to full Tx turn-up.
Transmitter output disable time		-	3	ms	Tx is in full turn-up state. The maximum transmitter turn-off time iscounted from assert Tx_disable pin
Transmitter turn-up time from cold start		-	90	s	Module is in Low_Power mode. The maximum Tx turn-up time is counted from de-assert the Low_power pin and Tx_disable pin to full Tx turn-up.
Transmitter OSNR		35		dB/0.1nm	OSNR at transmitter output (in-band)
Transmitter optical return loss		27	-	dB	
Transmitter output power with TX disabled			-40	dBm	
Transmitter polarization dependent power			1	dB	Power deference between X and Y polarization

Optical Receiver Specifications

Table 11 contains the general receiver specifications for 100G DP-QPSK/200G DP-16QAM oFEC.

Table 11: Optical Receiver Specifications with 100G DP-QPSK and 200G DP-16QAM at oFEC

Parameter	Typ.	Min	Max	Unit	Condition/comments
Receiver Frequency Range	193.7	191.3	196.10	THz	C band 50GHz ITU-T grid.
Input power range		-18	0	dBm	Signal power of the channel needed to meet the OSNR tolerance requirement
Receiver Sensitivity			-21	dBm	Minimum input power needed to achieve post FEC BER < 10-15 whenOSNR > 35dB and internal FEC enabled
OSNR Sensitivity @100G DP-QPSK	11.5		12.5	dB/0.1nm	At internal FEC threshold (post FEC BER < 10-15), at optimum Inputpower as specified above.
OSNR Sensitivity @200G DP-16QAM	19.5		21	dB/0.1nm	At internal FEC threshold (post FEC BER < 10-15), at optimum Inputpower as specified above.
Los assert			-29	dBm	
Los de-assert			-26	dBm	
Los hysteresis			3	dB	
CD Tolerance			40000	ps/nm	With less than 0.5dB OSNR penalty at FEC threshold.
DGD tolerance		50		ps	DGD tolerance Under the following conditions: 0.5dB OSNR penalty atFEC threshold;
PDL tolerance		3		dB	PDL tolerance under the following conditions:PDL applied before noise loading; Change in SOP is <=50rad/millisecond;With additional 1.5dB OSNR penalty
Tolerance to change in SOP		50	-	rad/ms	Tolerance to change in SOP with <0.5dB OSNR penalty at FEC threshold.
Input power transient tolerance		-2	2	dB	Optical input power transient tolerance Less than 0.5dB OSNR penaltyif the received power is within inout power range and rise/fall times of power change (defined by 20-80%) of 50μs or slower.
Input power reading accuracy		-1.5	1.5	dB	The module reports the actual power as received by the module.
Optical Return Loss		27		dB	
Receiver turn-up time from cold start		-	90	Seconds	Module is in Low_power state and valid Rx input signal is ready. The time from de-assert Low_power pin to full Rx turn-up, given that valid line side signal is ready.
RX LOS Assert time			3	ms	Assert Time of Receiver Loss of Signal
RX LOS De-assert time			3	ms	De-assert Time of Receiver Loss of Signal

Mechanical Overview & Dimensions

The CFP2 module is 107.5x41.5x12.4mm in size and is mechanically compliant to the requirements detailed the CFP2 Hardware Specification rev. 1.0. The module is designed to be inserted into a host board with a railing system that includes a heat sink.

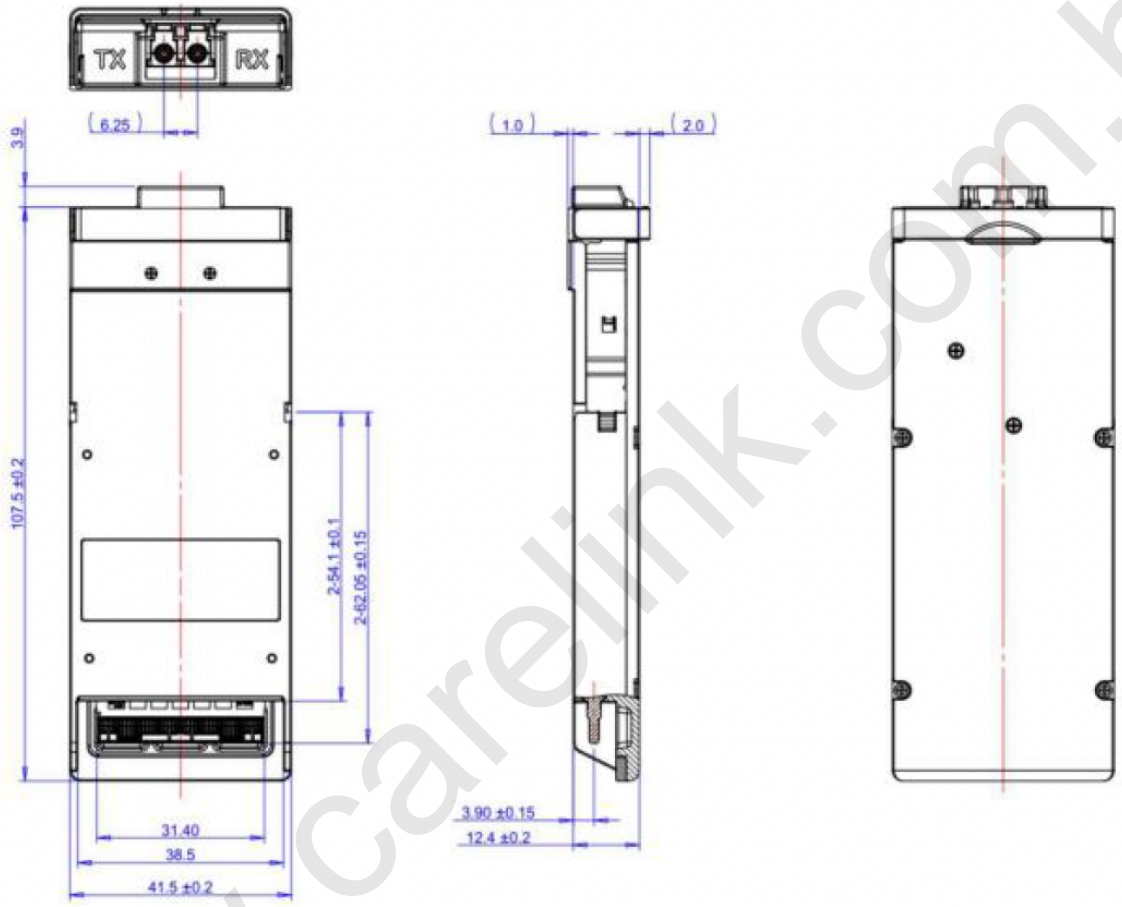

Figure 4: Mechanical Overview for CFP2

Host Electrical Connector & Pin Assignments

The module plug connector is a sub-component within the CFP2 module. The PCB inserts into the connector with a top and bottom row of pins (primary and secondary side PCB). The host connector has a physical offset of the pin contacts to ensure certain signals make and break contact before others. Ground mates first, the 3.3V and 3.3V ground mate second, the control and status signals mate third, and the MOD_LOPWR, MOD_ABS and high-speed data signals mate last. The module connector is a 104-pin plug connector and the connector pinout defined by the OIF-CFP2-DCO-01.0. All pins are showed as figure 5.

CFP2 Pin-Map

Pin Number	Name of Pin
1	GND
2	OHIO_RDn
3	OHIO_RDp
4	GND
5	OHIO_TDn
6	OHIO_TDp
7	3.3V GND
8	3.3V GND
9	3.3V
10	3.3V
11	3.3V
12	3.3V
13	3.3V GND
14	3.3V GND
15	VND_IO_A
16	VND_IO_B
17	PRG_CNTL1
18	PRG_CNTL2
19	PRG_CNTL3
20	PRG_ALRM1
21	PRG_ALRM2
22	PRG_ALRM3
23	GND
24	TX_DIS
25	RX_LOS
26	MOD_LOPWR
27	MOD_ABS
28	MOD_RSTn
29	GLB_ALRMn
30	GND
31	MDC
32	MDIO
33	PRTADR0
34	PRTADR1
35	PRTADR2
36	VND_IO_C
37	VND_IO_D
38	VND_IO_E
39	3.3V GND
40	3.3V GND
41	3.3V
42	3.3V
43	3.3V
44	3.3V
45	3.3V GND
46	3.3V GND
47	OHIO_REFCLKn
48	OHIO_REFCLKp
49	GND
50	TX_MCLKn
51	TX_MCLKp
52	GND

Pin Number	Name of Pin
104	GND
103	TX4n
102	TX4p
101	GND
100	TX3n
99	TX3p
98	GND
97	TX2n
96	TX2p
95	GND
94	TX5n
93	TX5p
92	GND
91	TX6n
90	TX6p
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	TX7n
81	TX7p
80	GND
79	(REFCLKn)
78	(REFCLKp)
77	GND
76	RX4n
75	RX4p
74	GND
73	RX3n
72	RX3p
71	GND
70	RX2n
69	RX2p
68	GND
67	RX5n
66	RX5p
65	GND
64	RX6n
63	RX6p
62	GND
61	RX1n
60	RX1p
59	GND
58	RX0n
57	RX0p
56	GND
55	RX7n
54	RX7p
53	GND

Figure 5: CFP2 4*56G or 8*28G bit/s pin-map

The bottom pins of module are descripted as following table.
Table 12: The pin description of Bottom

Pin Number	Name of Pin	Structure (Input/Output)	Logic	Description / Connection
1	GND	GND	Ground	
2	OHIO_RDn	O	CML	OHIO output: Differential 100Ω built-in,800-1200mVppd
3	OHIO_RDp	O	CML	OHIO output
4	GND	GND	Ground	
5	OHIO_TDn	I	CML	OHIO input: Differential 100Ω built-in,100-1200mVppd
6	OHIO_TDp	I	CML	OHIO input
7	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tiedtogether with Signal Ground
8	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tiedtogether with Signal Ground
9	3.3V	PWR	Power	3.3V Module Supply Voltage
10	3.3V	PWR	Power	3.3V Module Supply Voltage
11	3.3V	PWR	Power	3.3V Module Supply Voltage
12	3.3V	PWR	Power	3.3V Module Supply Voltage
13	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tiedtogether with Signal Ground
14	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tiedtogether with Signal Ground
15	VND_IO_A	I/O	LVCMOS	TXD0 of Uart0 (For FPGA: Module to PC)
16	VND_IO_B	I/O	LVCMOS	RXD0 of Uart0 (For FPGA: PC to Module)
17	PRG_CNTL1	I	LVCMOS w/PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled or notused
18	PRG_CNTL2	I	LVCMOS w/PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB,"00": ≤9W, "01": ≤12W, "10": ≤ 15W, "11" or NC: ≤18W or not used
19	PRG_CNTL3	I	LVCMOS w/PUR	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB,"00": ≤9W, "01": ≤12W, "10": ≤15W, "11" or NC:≤18W or not used
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1; MSA Default “H” = HIPWR_ON
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2; MSA Default “H” = MOD_READY
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3; MSA Default “H” = MOD_FAULT
23	GND	GND	Ground	
24	TX_DIS	I	LVCMOS w/PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" =transmitter enabled
25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal

				condition
26	MOD_LOPWR	I	LVCMOS w/PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0":power-on enabled
27	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, PullUp Resistor on Host
28	MOD_RSTn	I	LVCMOS w/PUR	Module Reset. "0" resets the module, "1" or NC = module enabled, PullDown Resistor in Module
29	GLB_ALRMn	O	LVCMOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarmcondition, Open Drain, Pull Up Resistor on Host
30	GND	GND	Ground	
31	MDC	I	1.2V LVCMOS	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)
32	MDIO	I/O	1.2V LVCMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std802.3-2012)
33	PRTADR0	I	1.2V LVCMOS	MDIO Physical Port Address bit 0
34	PRTADR1	I	1.2V LVCMOS	MDIO Physical Port Address bit 1
35	PRTADR2	I	1.2V LVCMOS	MDIO Physical Port Address bit 2
36	VND_IO_C	I/O	LVCMOS	TMS/SWDIO (PC to Module or Module to PC)
37	VND_IO_D	I	LVCMOS	TCK/SWDCK (PC to Module)
38	VND_IO_E	I/O	LVCMOS	TXD1 of Uart1 (Module to PC)
39	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply returnpath.
40	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply returnpath.
41	3.3V	PWR	Power	3.3V power supply
42	3.3V	PWR	Power	3.3V power supply
43	3.3V	PWR	Power	3.3V power supply
44	3.3V	PWR	Power	3.3V power supply
45	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply returnpath.
46	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. powersupply return path.
47	OHIO_REFCLKn	I	CML	OHIO ref clk input,100MHz, ±100 ppm，100-1200mVppd
48	OHIO_REFCLKp	I	CML	OHIO ref clk input,Differential 100Ω built-in
49	GND	GND	Ground	Module Ground. Logic and power return path
50	TX_MCKLn	O	CML	TX lineside monitor clock
51	TX_MCKLn	O	CML	TX lineside monitor clock
52	GND	GND	Ground	Module Ground. Logic and power return path

Table 13: The pin description of Top

Pin#	Name				Description
	4x28GNRZ	8x28G NRZ	2x56GPAM4	4x56GPAM4	
104	GND	GND	GND	GND	Ground
103	N.C.	TX4n	N.C.	N.C.	Transmitter lane 4
102	N.C.	TX4p	N.C.	N.C.	
101	GND	GND	GND	GND	Ground
100	TX3n	TX3n	N.C.	TX3n	Transmitter lane 3
99	TX3p	TX3p	N.C.	TX3p	
98	GND	GND	GND	GND	Ground
97	TX2n	TX2n	N.C.	TX2n	Transmitter lane 2
96	TX2p	TX2p	N.C.	TX2p	
95	GND	GND	GND	GND	Ground
94	N.C.	TX5n	N.C.	N.C.	Transmitter lane 5
93	N.C.	TX5p	N.C.	N.C.	
92	GND	GND	GND	GND	Ground
91	N.C.	TX6n	N.C.	N.C.	Transmitter lane 6
90	N.C.	TX6p	N.C.	N.C.	
89	GND	GND	GND	GND	Ground
88	TX1n	TX1n	TX1n	TX1n	Transmitter lane 1
87	TX1p	TX1p	TX1p	TX1p	
86	GND	GND	GND	GND	Ground
85	TX0n	TX0n	TX0n	TX0n	Transmitter lane 0
84	TX0p	TX0p	TX0p	TX0p	
83	GND	GND	GND	GND	Ground
82	N.C.	TX7n	N.C.	N.C.	Transmitter lane 7
81	N.C.	TX7p	N.C.	N.C.	
80	GND	GND	GND	GND	Ground
79	(REFCLKn)	(REFCLKn)	(REFCLKn)	(REFCLKn)	N.C
78	(REFCLKp)	(REFCLKp)	(REFCLKp)	(REFCLKp)	
77	GND	GND	GND	GND	Ground
76	N.C.	RX4n	N.C.	N.C.	Receiver lane 4
75	N.C.	RX4p	N.C.	N.C.	
74	GND	GND	GND	GND	Ground

73	RX3n	RX3n	N.C.	RX3n	
72	RX3p	RX3p	N.C.	RX3p	Receiver lane 3
71	GND	GND	GND	GND	Ground
70	RX2n	RX2n	N.C.	RX2n	Receiver lane 2
69	RX2p	RX2p	N.C.	RX2p	
68	GND	GND	GND	GND	Ground
67	N.C.	RX5n	N.C.	N.C.	Receiver lane 5
66	N.C.	RX5p	N.C.	N.C.	
65	GND	GND	GND	GND	Ground
64	N.C.	RX6n	N.C.	N.C.	Receiver lane 6
63	N.C.	RX6p	N.C.	N.C.	
62	GND	GND	GND	GND	Ground
61	RX1n	RX1n	RX1n	RX1n	Receiver lane 1
60	RX1p	RX1p	RX1p	RX1p	
59	GND	GND	GND	GND	Ground
58	RX0n	RX0n	RX0n	RX0n	Receiver lane 0
57	RX0p	RX0p	RX0p	RX0p	
56	GND	GND	GND	GND	Ground
55	N.C.	RX7n	N.C.	N.C.	Receiver lane 7
54	N.C.	RX7p	N.C.	N.C.	
53	GND	GND	GND	GND	Ground

The differents of High-speed Pin-Map for 100G/200G application

For 100G application, there are two interface modes: 4*28G NRZ, which can be supported: 1*CAUI-4, 1* OTL4.4. For 200G application, there are two interface modes: 8*28G NRZ, which can be supported: 2*CAUI-4, 2* OTL4.4.

Table 14: The pin-map of High-speed pin for 100G/200G application

SerDes Lanes	**200G**	**100G**
	2*CAUI-4 2*OTL4.4 (NRZ)	**1*CAUI-4 1*OTL4.4 (NRZ)**
	Interface - CH[x,y]	
Tx7[p,n];Rx7 [p,n]	CH2.2	NC

Tx6[p,n];Rx6 [p,n]		
Tx5[p,n];Rx5 [p,n]		
Tx4[p,n];Rx4 [p,n]		
Tx3[p,n];Rx3 [p,n]	CH2.1	CH1.1
Tx2[p,n];Rx2 [p,n]		
Tx1[p,n];Rx1 [p,n]		
Tx0[p,n];Rx0 [p,n]		

Note:
1.The CFP2 Host/Client interface naming convention is CH, where, CH=Channel,
2.<x>.<y>:
<x> = channel capacity, where [x=1,2] is 1=100G or 2=200G.
<y> = channel numeration, where [y=1 …3] is channel numeration.
3.NC –No connected

Glossary

Glossary	Info.
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BS	Beam Splitter
CMRR	Common Mode Rejection Ratio
DSP	Digital Signal Processor
IA	Implementation Agreement
LO	Local Oscillator
MGC	Manual Gain Control
MPD	Monitor Photodiode
MSA	Multi-Source Agreement
OIF	Optical Internetworking Forum
PBS	Polarization Beam Splitter
PCB	Printed Circuit Board
DP-QPSK	Dual Polarization Quadrature Phase Shift Keying
DP-16QAM	Dual Polarization Quadrature Amplitude Modulation
OTU4	Optical Transport channel Uint-4
CD	Chromatic Dispersion
PDL	Polarization Dependent Loss
SOP	State of Polarization

DGD	Differential Group Delay
SOPMD	Second Order Polarization Mode Dispersion

Reference Documents

1.OIF-CFP2-DCO-01.0, Implementation Agreement for CFP2-Digital Coherent Optics Module, October 17, 2018
2.CFP2_HW-Spec-rev1.0, July 31, 2013.
1.OIF-CFP2-DCO-01.0, Implementation Agreement for CFP2-Digital Coherent Optics Module, October 17, 2018
2.CFP2_HW-Spec-rev1.0, July 31, 2013.
3.OIF-CEI-04.0, December 29, 2017
4.IEEE P802.3bm, 40Gbit/s and 100Gbit/s Operation Over Fiber Optic Cables Task Force, http://www.ieee802.org/3/bm/index.html
5.ITU-T Recommendation G.709 (2012) Interfaces for the Optical Transport Network (OTN).
6.IEEE Std 802.3TM-2012, Annexes 83A, 83B, and 86A.
7.CFP MSA Management Interface Specification, Version 2.6 r06a, March 27, 2017.
8.IEEE Std 802.3TM-2012, Cl. 45, Management Data Input/output (MDIO) Interface.
9.CFP2 MSA CFP/CFP/CFP4 Pin Allocation Rev. 25
10.KR4-FEC: KR4-FEC for 100GbE Client RS(528, 514) -- IEEE802.3 standard Refer to Clause 74, 91
11.KP4-FEC: KP4-FEC for 100GbE/200GbE/400GbE Client RS(544, 514) -- IEEE802.3 standard Refer to Clause 91, 119
12.RS10: FlexO FEC RS10(544, 514) -- ITU-T G.709.1
13.OIF FlexE IA: OIF, Flex Ethernet Implementation Agreement (2016)
14.oFEC: OpenRoadm FEC -- Open ROADM MSA specification ver.3.00, Filename:20181217a Open ROAD MSA specification ver 3 00

ESD

This transceiver is specified as ESD threshold 500V for according to GR-78 (Human Body Model) on the high speed pins and 2000v for all others electrical pins. However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

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