



RoHS compliant
850 nm Multi-mode XENPAK Transceiver
10GBASE-SR(Ethernet)



Features

- Compatible to IEEE802.3ae 10GBASE-SR at 10.3125 Gb/s
- Up to 8m transmission on 62.5/125 μm MMF (<2000 MHz km)
- Up to 300m transmission on 50/125 μm MMF (<500 MHz km)
- Laser Class 1 compliant
- Hot-Pluggable 70 pin connector with XAUI interface
- Alarms, controls and performance monitoring
- VCSEL laser
- Duplex SC connector interface
- Compliant with the EU RoHS 6 Environmental Requirements

Introduction

The CL-XENPAK10GB-SR is a highly integrated, serial optical transponder module for high-speed, 10Gbit/s data transmission applications. The module is fully compliant to IEEE 802.3ae standard for Ethernet making it ideally suited for 10 GbE applications. The modules operate at 850nm and is designed for distances of up to 300m. The transceiver module comprises a VCSEL laser transmitter, a receiver with a PIN photodiode, a XAUI-Attachment Interface, an integrated Coder / Decoder and multiplexer / demultiplexer (SERDES: Serializer / Deserializer). The transceiver operates within a wide temperature range of 0°C ~ 70°C and offers optimum heat dissipation and excellent electromagnetic shielding. A 70 pin electrical connector and a duplex SC connector optical interface assure the XENPAK MSA compliant connectivity.

Applications

- IEEE802.3ae 10GBASE-SR 10.3125Gb/s
- Inter and Intra
- Data Centers

Ordering Information

Model Number	Wavelength	TX Power (dBm)	Receiver Sensitivity (dBm)	Reach
CL-XENPAK10GB-SR	850nm	-1~ -7.5	-1~ -9.9	300m

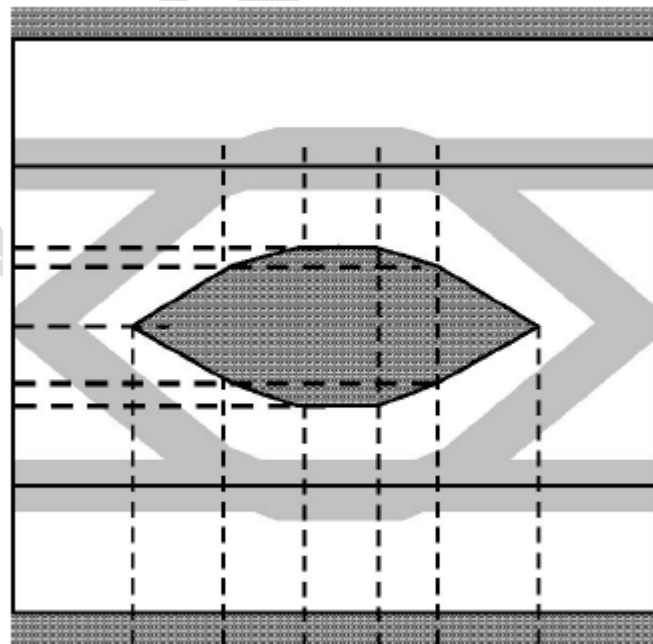


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Optical Characteristics

Table 1. Optical Characteristics

No.	Parameters	Symbols	Min.	Typ.	Max.	Unit	Remarks
1	Center Wavelength	λ_c	840	850	860	nm	
2	Signaling speed		-	10.3125	-	Gbit/s	
3	Signaling speed variation from nominal		-100	-	+100	ppm	
4	Optical modulation amplitude	OMA	-5.2	-	-	dBm	Note 1
5	Optical Output Power	P_f	-7.3	-	-1.3	dBm	Average
6	Optical Waveform	-					
7	Side Mode Suppression Ratio	S_r	30	-	-	dB	Average
8	Extinction Ratio	E_r	3.0	-	-	dB	
9	Off Transmit Power	P_{off}	-	-	-30	dBm	Average
10	Optical Output turn-off Time	TTX-OFF	-	-	100	μs	Figure10
11	Receiver Sensitivity in OMA	OMArmin		-	-11.1	dBm	
12	Receiver Overload	R_{to}	+0.5	-	-	dBm	Average
13	Receiver Return Loss	RL	12	-	-	dB	Average





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Table2. Power Supply Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Supply Voltage	VCC1	3.135	3.300	3.465	V	
2	Supply Voltage	VCC2	1.152	1.200	1.248	V	
3	Supply Current	ICC1	-	-	1.4	A	+3.3 V
4	Supply Current	ICC2	-	-	1.7	A	APS
5	Power Consumption	PDS	-	-	2.2	W	
6	Power supply stabilization time	TDF	-	-	500	ms	Figure 7
7	Initialization Time	TINIT	-	-	5	s	Figure 7
8	RESET Assert Time	TRESET	1	-	-	ms	Figure 9
9	Hold Time after rising edge of RESET	THOLD	500	-	-	ms	Figure 9

Table 3. XAUI Driver Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Baud Rate		-	3.125	-	Gbit/s	
2	Baud Rate Tolerance		-100	-	+100	ppm	
3	Differential Amplitude		800	-	1600	mV _{PP}	AC, near-end value



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Table4. 1.2VCMOS Interface Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Baud Rate		-	3.125	-	Gbit/s	
2	Baud Rate Tolerance		-100	-	+100	ppm	
3	Differential Amplitude		200	-	1600	mVpp	AC

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Input High Voltage	V _{IH}	0.84	-	1.5	V	
2	Input Low Voltage	V _{IL}	-0.3	-	0.36	V	
3	Input Pull-down Current	I _{in}	20	40	120	μA	V _{IH} =1.2V
4	Output High Voltage	V _{OH}	1.0	-	-	V	Pull-up=10k ohm to 1.2V
5	Output Low Voltage	V _{OL}	-	-	0.2	V	
6	Pull up Resistance	R _{LAS1}	10	-	22	k ohm	Figure 8
7	Capacitance	C _{LAS1}	-	-	10	pF	Figure 8
8	Load Capacitance	C _{Load}	-	-	320	pF	Figure 8

Table5. MDIO Bidirectional Interface Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Input High Voltage	V _{IHM}	0.84	-	1.5	V	
2	Input Low Voltage	V _{ILM}	-0.3	-	0.36	V	
3	Output High Voltage	V _{OHM}	1.0	-	1.5	V	
4	Output Low Voltage	V _{OLM}	-0.3	-	0.2	V	
5	Pull up Resistance	R _{MDIO}	200	-	Note 1	Ohm	Figure 5
6	MDC min high/low time	T _{HM} , T _{LM}	160	-	-	ns	Figure 3
7	MDC Frequency	1/T _{CK}	TBD	-	2.5	MHz	
8	Setup time	T _{DIS}	10	-	-	ns	Figure 3
9	Hold time	T _{DIH}	10	-	-	ns	Figure 3
10	MDIO output delay after rising edge of MDC	T _{PD}	0	-	300	ns	Figure 4
12	Input Capacitance	C _i	-	-	10	pF	Figure 5
13	Bus Loading	C _L	-	-	470	pF	Figure 5

Note 1 : The maximum value of R_{MDIO} depends on bus loading(C_L) , input capacitance(C_i), and MDC frequency(1/T_{CK}).



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70	GND	1	GND
69	GND	2	GND
68	RESERVED	3	GND
67	RESERVED	4	RESERVED
66	GND	5	3.3V
65	TX LANE3	6	3.3V
64	TX LANE3+	7	APS
63	GND	8	APS
62	TX LANE2	9	LASI
61	TX LANE2+	10	RESET
60	GND	11	VEND SPECIFIC
59	TX LANE1	12	TX ON/OFF
58	TX LANE1+	13	RESERVED
57	GND	14	MOD DETECT
56	TX LANE0	15	VEND SPECIFIC
55	TX LANE0+	16	VEND SPECIFIC
54	GND	17	MDIO
53	GND	18	MDC
52	GND	19	PRTAD4
51	RX LANE3	20	PRTAD3
50	RX LANE3+	21	PRTAD2
49	GND	22	PRTAD1
48	RX LANE2	23	PRTAD0
47	RX LANE2+	24	VEND SPECIFIC
46	GND	25	APS SET
45	RX LANE1	26	RESERVED
44	RX LANE1+	27	APS SENSE
43	GND	28	APS
42	RX LANE0	29	APS
41	RX LANE0+	30	3.3V
40	GND	31	3.3V
39	RESERVED	32	RESERVED
38	RESERVED	33	GND
37	GND	34	GND
36	GND	35	GND



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Figure 1 XENPAK Pin Configuration

Pin #	Symbol	I/O	Logic	Description	Notes
1	GND	I	Supply	Electrical ground	
2	GND	I	Supply	Electrical ground	
3	GND	I	Supply	Electrical ground	
4	RESERVED	-	-	Reserved	
5	3.3 V	I	Supply	Power	
6	3.3 V	I	Supply	Power	
7	APS	I	Supply	Adaptive Power Supply	
8	APS	I	Supply	Adaptive Power Supply	
9	LASI	O	Open Drain	Link Alarm Status Interrupt. 10-22k ohm pull up on host.	
10	RESET	I	1.2V CMOS	TX OFF when MDIO RESET	
11	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
12	TX ON/OFF	I	1.2V CMOS	Transmitter ON/OFF	
13	RESERVED	-	-	Reserved	
14	MOD DETECT	O	-	Pulled low inside module through 1k ohm.	
15	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	



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Pin #	Symbol	I/O	Logic	Description	Notes
16	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
17	MDIO	I/O	Open Drain	Management Data IO	
18	MDC	I	1.2V CMOS	Management Data Clock	
19	PRTAD4	I	1.2V CMOS	Port Address bit 4 (Low=0)	
20	PRTAD3	I	1.2V CMOS	Port Address bit 3 (Low=0)	
21	PRTAD2	I	1.2V CMOS	Port Address bit 2 (Low=0)	
22	PRTAD1	I	1.2V CMOS	Port Address bit 1 (Low=0)	
23	PRTAD0	I	1.2V CMOS	Port Address bit 0 (Low=0)	
24	VEND SPECIFIC	-	-	Vendor Specific Pin. Leave unconnected.	
25	APS SET	O	-	Feedback output for APS	
26	RESERVED	-	-	Reserved for Avalanche Photodiode use.	
27	APS SENSE	O	Analog	APS Sense Connection	
28	APS	I	Supply	Adaptive Power Supply	
29	APS	I	Supply	Adaptive Power Supply	
30	3.3 V	I	Supply	Power	
31	3.3 V	I	Supply	Power	
32	RESERVED	-	-	Reserved	
33	GND	I	Supply	Electrical Ground	
34	GND	I	Supply	Electrical Ground	
35	GND	I	Supply	Electrical Ground	

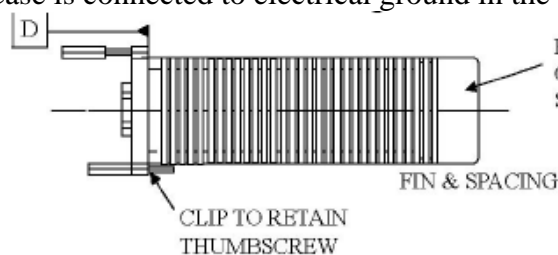
Pin #	Symbol	I/O	Logic	Description	Notes
36	GND	I	Supply	Electrical Ground	
37	GND	I	Supply	Electrical Ground	
38	RESERVED	-	-	Reserved	
39	RESERVED	-	-	Reserved	



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40	GND	I	Supply	Electrical Ground	
41	RX LANE 0+	O	AC	Module XAUI Output Lane 0+	
42	RX LANE 0-	O	AC	Module XAUI Output Lane 0-	
43	GND	I	Supply	Electrical Ground	
44	RX LANE 1+	O	AC	Module XAUI Output Lane 1+	
45	RX LANE 1-	O	AC	Module XAUI Output Lane 1-	
46	GND	I	Supply	Electrical Ground	
47	RX LANE 2+	O	AC	Module XAUI Output Lane 2+	
48	RX LANE 2-	O	AC	Module XAUI Output Lane 2-	
49	GND	I	Supply	Electrical Ground	
50	RX LANE 3+	O	AC	Module XAUI Output Lane 3+	
51	RX LANE 3-	O	AC	Module XAUI Output Lane 3-	
52	GND	I	Supply	Electrical Ground	
53	GND	I	Supply	Electrical Ground	
54	GND	I	Supply	Electrical Ground	
55	TX LANE 0+	I	AC	Module XAUI Input Lane 0+	
56	TX LANE 0-	I	AC	Module XAUI Input Lane 0-	
57	GND	I	Supply	Electrical Ground	
58	TX LANE 1+	I	AC	Module XAUI Input Lane 1+	
59	TX LANE 1-	I	AC	Module XAUI Input Lane 1-	
60	GND	I	Supply	Electrical Ground	
61	TX LANE 2+	I	AC	Module XAUI Input Lane 2+	
62	TX LANE 2-	I	AC	Module XAUI Input Lane 2-	
63	GND	I	Supply	Electrical Ground	
64	TX LANE 3+	I	AC	Module XAUI Input Lane 3+	
65	TX LANE 3-	I	AC	Module XAUI Input Lane 3-	
66	GND	I	Supply	Electrical Ground	
67	RESERVED	-	-	Reserved	
68	RESERVED	-	-	Reserved	
69	GND	I	Supply	Electrical Ground	
70	GND	I	Supply	Electrical Ground	

Note: Case is connected to electrical ground in the module.





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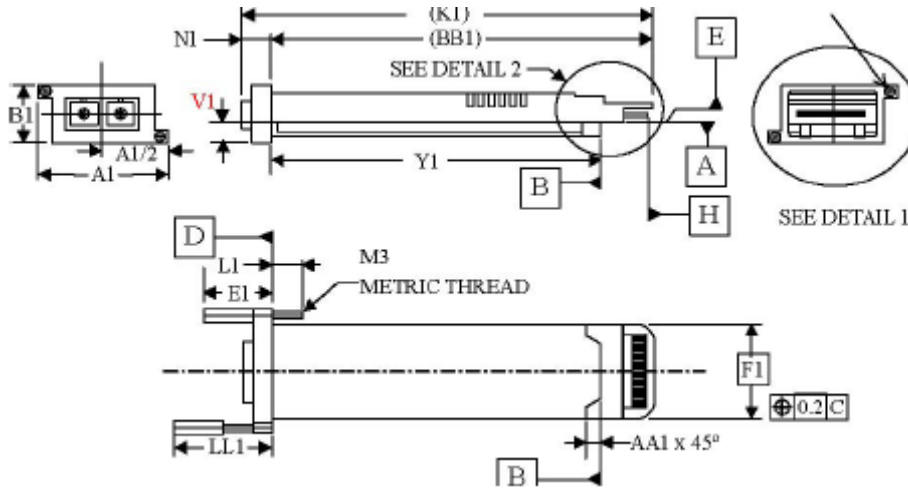


Figure 2 Mechanical dimensions Refer to Table 10 for Dimensions

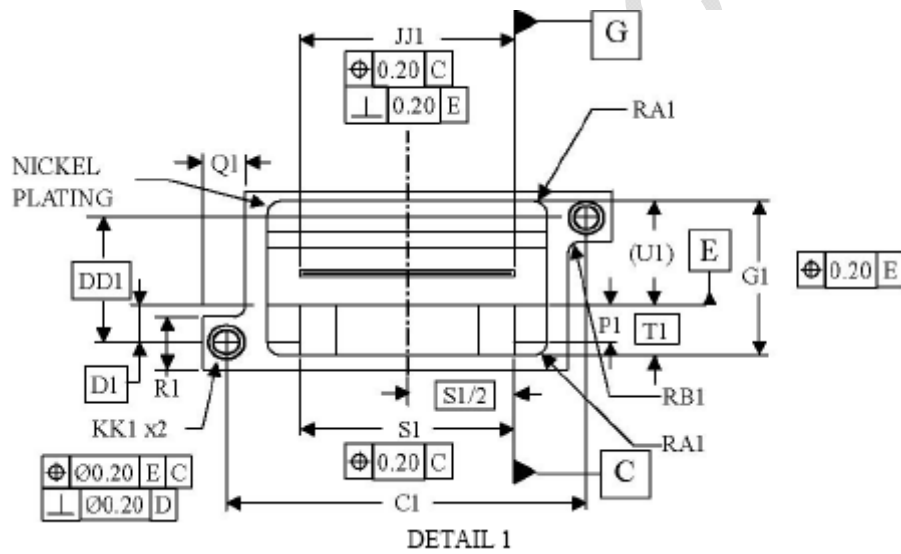


Figure 3 Mechanical dimensions of End View of Transceiver



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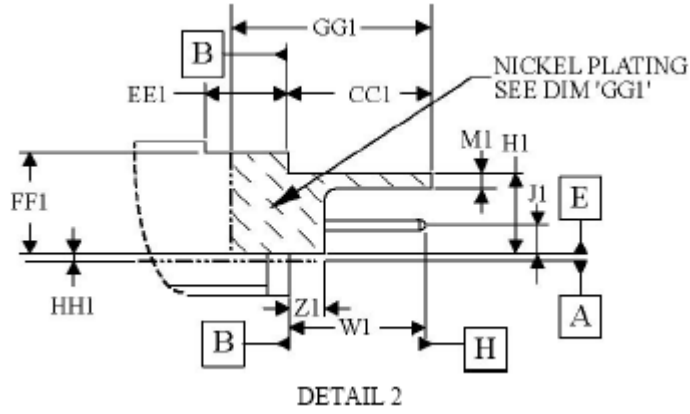


Figure 4 Mechanical dimensions of Side Elevation Transceiver

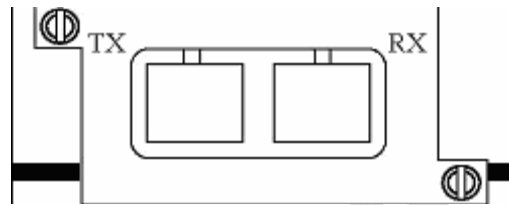


Figure 5 Orientation Keying of TX and RX Orientation Vs PCB



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Table 7 Package Dimensions Table11 Definition of Datums

KEY	VALUE, mm / inch	TOLERANCE mm	COMMENTS
A1	51.3 2.020	±0.20	Width of Bezel overall
B1	22.4 0.882	±0.20	Height of Bezel overall
C1	45.5 1.791	BASIC	Distance between captive screws in 'X' axis (Horizontal)
D1	3.7 0.136	BASIC	Datum 'E' to lower captive screw
E1	20.75 0.817	Maximum	Extension of captive screw
F1	36.0 1.417	±0.20	Width of Transceiver body
G1	17.4 0.685	±0.20	Height of Transceiver body
H1	8.15 0.321	±0.20	Datum 'E' to top of Over-hanging Ledge
J1	3.05 0.120	±0.25	Datum 'E' to centerline of Transceiver PCB
K1	(121.0) 4.764	REF	Length of Transceiver overall minus protruding captive screw heads
L1	5.00 0.197	±0.20	Length of captive screw from Datum 'D' to end of threaded end
M1	1.5 0.059	±0.20	Thickness of Over-hanging Ledge
N1	5.8 0.228	±0.20	Datum 'D' to front of Transceiver Bezel
P1	4.07 0.160	Minimum	Slot or channel formed by Interposer to accommodate Customers PCB range. Use of an Interposer spring is not a requirement of this specification.
Q1	4.65 0.183	±0.20	Protrusion of side flange on Transceiver Bezel
R1	7.12 0.280	±0.20	Height of side flange on Transceiver Bezel
S1	29.5 1.161	±0.20	Width of Transceiver slot to accommodate rail or Customers PCB
T1	5.42 0.213	BASIC	Datum 'E' to bottom of Transceiver
U1	(11.98) 0.472	REF	Datum 'E' to top of Transceiver
V1	7.92 0.312	±0.20	Datum 'E' to bottom of Transceiver Bezel
W1	11.10 0.437	±0.20	Datum 'B' to end of protruding Transceiver PCB
Y1	102.20 4.024	±0.20	Datum 'D' to Datum 'B'
Z1	4.0 0.157	±0.20	Datum 'B' to end of side protective shroud to mate with EMI/Conn. Shield
AA1	3.0 0.118	±0.50	Datum 'B' to end of 45° chamfer
BB1	(115.2) 4.535	REF	Length of Module from Datum 'D' to rear Over-hanging Ledge
CC1	13.0 0.512	±0.50	Datum 'B' to end of Over-hanging Ledge for EMI Plating
DD1	13.96 0.550	BASIC	Distance between captive screws in 'Y' axis (Vertical)
EE1	10.0 0.394	Minimum	Datum 'B' end of recess for insertion clearance
FF1	10.48 0.422	±0.50	Datum 'E' to top of recess for insertion clearance
GG1	20.0 0.787	Minimum	Length of Transceiver side wall for EMI plating
HH1	0.25 0.01	BASIC	Datum 'A' to Datum 'E'



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JJ1	29.2 1.150	±0.10	Width of Transceiver PCB
KK1	3.0 0.118	N/A	Hole for 3mm screw Thumbscrew, tapped or clearance
LL1	25.8 1.016	Maximum	Length of Thumbscrew
RA1	1.25 0.049	Minimum	External radius or chamfer of Transceiver
RB1	1.5 0.059	Maximum	Internal radius or chamfer on exterior flange of Transceiver Bezel

DATUM	DESCRIPTION TRANSCEIVER/LINECARD
A	CUSTOMERS PCB TOP SURFACE
B	PHYSICAL HARD STOP FOR TRANSCEIVER
C	EDGE OF TRANSCEIVER SLOT
D	BACK SURFACE OF TRANSCEIVER BEZEL, SAFETY HARD STOP
E	TRANSCEIVER TOP SURFACE OF SLOT 'P1'
F	FRONT SURFACE OF CUSTOMERS FACEPLATE
G	EDGE OF TRANSCEIVER'S PCB
H	LEADING EDGE OF TRANSCEIVER PCB
J	EDGE OF CUT-OUT IN CUSTOMER'S PCB
K	PHYSICAL HARD STOP ON CUSTOMER'S PCB

Optical connector

No.	Parameter	Specifications	Remarks
1	SC Duplex Receptacle	IEC61754-4	Optical bores 12.25/13.15mm
2	SC Duplex plug	IEC61754-4	Optical bores 12.25/13.15mm