

CL-MC-XE1-IP TDM over IP Converter, Framed & Unframed, up to 4 and \*8 E1 channels, Telnet & Web Management



# \*2G/3G/4G BACKHAUL DEPLOYMENT

With high precision clock recovery technology, CL-MC-XE1-IP is capable of supporting 2G/3G/4G backhaul and provides smooth services.

## Owerview

CL-MC-XE1-IP - is designed as a multiservice access platform for E1 over IP applications. E1 frames can be mapped/demapped into/from IP packets. An adaptive clock recovery method for Ingress PDH (PSN -> TDM) clock generation is implemented to support E1 (ITU-T G.823) Jitter performance.

**COST-EFFECTIVE LAN DEPLOYMENT** (PDH OVER ETHERNET) CL-MC-XE1-IP provides cost-effective applications of traditional circuitswitched system over IP. With CL-MC-XE1-IP, it is easy to interconnect with the existing E1 systems over IP that are used to carry data, voice and video.

**TRANSPARENT TRANSMISSION CL-MC-XE1-IP** can transparently transport proprietary signaling that is required to support PABX & IP-PABX features, including call conference, call forwarding and SS7. Customer can

easily apply and enjoy better integration of TDM and Ethernet devices with lower network expense.

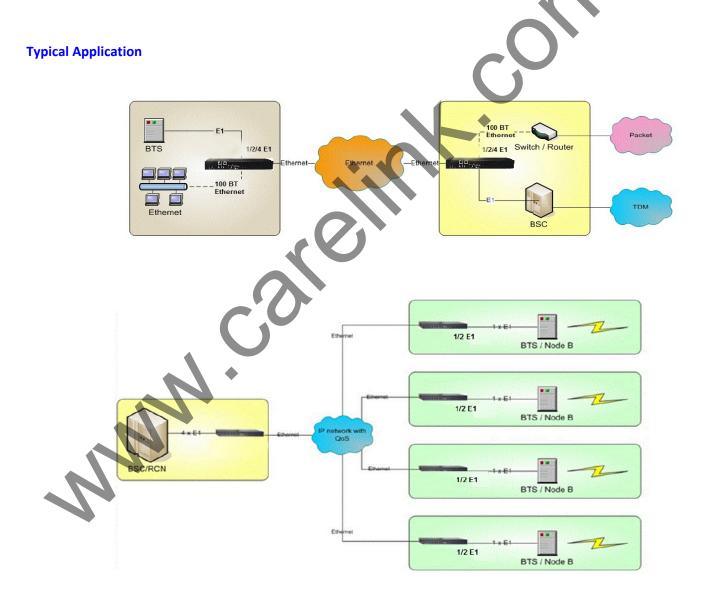
**BYPASS INTERNATIONAL TOLL** With a pair of EtherMux and guaranteed internet bandwidth, it is sure to save cost dramatically, and to ensure the QoS of voice based on interconnections of TDM telecommunications equipment

## Features

- Support IEFT RFC4533 Structure Agnostic TDM over Packet(SAToP), Metro Ethernet Forum MEF8.
- ET NRZ Serial Interface with LOS/AIS detection.
- Use Raw Encapsulation method for PDH payload over Ethernet packet.
- Support Circuit Emulation Service over Ethernet networks.
- Comply with IEFT draft standard for CESoPSN and SAToP; Metro Ethernet Forum MEF8 IA.
- Support both Point-to-Point and Point-to-Multipoint operation.
- Support Adaptive Clock recovery block for Ingress PDH (PSN ->TDM) clock generation.
- Recovered clock jitter is compliant to ITU-T G.823 (E1 Jitter Control).

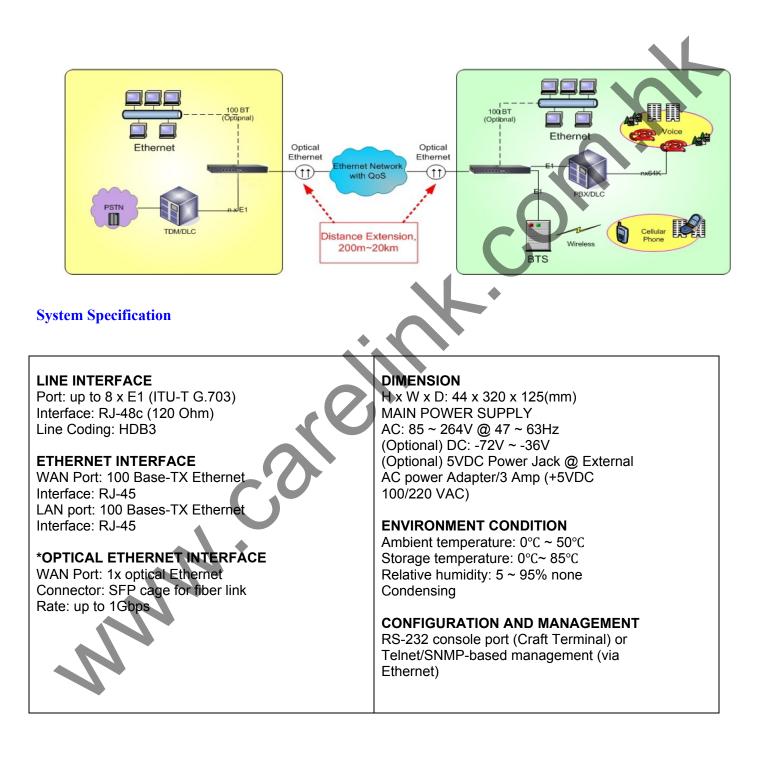


- Configurable jitter buffer depth to compensate PDV (Packet Delay Variation) with the flexible setting of 11ms, 23ms, 40ms, 75 ms...
- Lost packets processing/compensation via PW (Pseudo Wire) control field Sequence Number.
- Provide Subscriber side Data traffic bandwidth control to guarantee enough TDM payload bandwidth.
- PDH LOS detection triggered PW L field or payload AIS generation at Egress direction (TDM -> PSN).
- Configurable IEEE 802.3 DA/SA assignment.
- LED alarm display for E1 /Power failure status (Optional) Order wire (free contact)





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### **Order Information**

#### **Part Number**

CL-MC-1E1-IP-A 1E1 over 1 Ethernet pot, Standalone, AC220V power supply CL-MC-1E1-IP-D 1E1 over 1 Ethernet pot, Standalone, DC-48V power supply CL-MC-2E1-IP-A 2E1 over 1 Ethernet pot, Standalone, AC220V power supply CL-MC-2E1-IP-D 2E1 over 1 Ethernet pot, Standalone, DC-48V power supply CL-MC-4E1-IP-A 4E1 over 1 Ethernet pot, Standalone, AC220V power supply CL-MC-4E1-IP-D 4E1 over 1 Ethernet pot, Standalone, DC-48V power supply \*CL-MC-8E1-IP-A 8E1 over 1 Ethernet pot, Standalone, AC220V power supply \*CL-MC-8E1-IP-D 8E1 over 1 Ethernet pot, Standalone, DC-48V power supply

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